What is claimed is:

1. A synchronous flash memory device comprising:
   an array of non-volatile memory cells; and
   a plurality of external connections comprising,
      a plurality of bi-directional data connections,
      a plurality of memory address connections,
      a clock input connection,
      a write enable connection,
      a column address strobe connection, and
      a row address strobe connection.

2. The synchronous flash memory device of claim 1, wherein the plurality of external connections further comprises:
   a clock enable connection,
   a chip select connection,
   a plurality of memory array bank address connections,
   power supply connections,
   a plurality of data mask connections, and
   a reset connection.

3. The synchronous flash memory device of claim 1, wherein the plurality of external connections further comprises a Vccp power supply connection.

4. The synchronous flash memory device of claim 1, further comprising a package having a plurality of interconnect pins corresponding to the external connections.

5. The synchronous flash memory device of claim 4, wherein the interconnect pins are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

6. The synchronous flash memory device of claim 1, further comprising a package having a plurality of conductive interconnect locations corresponding to the external connections.

7. The synchronous flash memory device of claim 6, wherein the conductive interconnect locations are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

8. The synchronous flash memory device of claim 7, wherein the synchronous flash memory device operates within read timing specification parameters for an SDRAM.

9. A synchronous flash memory device comprising:
an array of non-volatile memory cells; and
a package having a plurality of interconnect pins arranged in a manner that corresponds to interconnect pins of a synchronous dynamic random access memory device, wherein the plurality of interconnect pins of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) interconnect pins of the synchronous dynamic random access memory.

10. The synchronous flash memory device of claim 9, wherein the plurality of interconnect pins comprises:
a plurality of bi-directional data connections,
a plurality of memory address connections,

a write enable connection,

a clock input connection,

a column address strobe connection,

a row address strobe connection, and

power supply connections.

11. The synchronous flash memory device of claim 10, wherein the plurality of interconnect pins further comprises:

a clock enable connection,

a chip select connection,

a plurality of memory array bank address connections,

a plurality of data mask connections,

a reset connection, and

a Vccp power supply connection.

12. A synchronous flash memory device comprising:

an array of non-volatile memory cells; and

a package having a plurality of solder bump connections arranged in a manner that corresponds to solder bump connections of a synchronous dynamic random access memory device, wherein the plurality of solder bump connections of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) solder bump connections of the synchronous dynamic random access memory.

13. The synchronous flash memory device of claim 12, wherein the plurality of solder bump connections comprises:

a plurality of bi-directional data connections,

a plurality of memory address connections,

a write enable connection,

a clock input connection,

a column address strobe connection,

a row address strobe connection, and

power supply connections.

14. The synchronous flash memory device of claim 13, wherein the plurality of interconnect pins further comprises:

a clock enable connection,

a chip select connection,

a plurality of memory array bank address connections,

a plurality of data mask connections,

a reset connection, and

a Vccp power supply connection.

15. A synchronous flash memory device having an interface comprising:

a clock input connection (CLK) to receive a clock signal;

a write enable connection (WE#) to receive a write enable signal;

a column address strobe connection (CAS#) to receive a column address strobe signal;

a row address strobe connection (RAS#) to receive a row address strobe signal;

a chip select connection (CS#) to receive a chip select signal;

a reset connection (RP#) to receive a reset signal; and

a Vccp power supply connection to receive an elevated power supply signal.

16. The synchronous flash memory device of claim 15, wherein the interface further comprises:

a plurality of bi-directional data connections (DQ);

a plurality of memory address connections;

a clock enable connection (CKE);

a plurality of memory array bank address connections (BA#);

power supply connections (Vcc and Vss); and

a plurality of data mask connections (DQM).

17. The synchronous flash memory device of claim 16, further comprising a package having a plurality of interconnect pins corresponding to the command interface connections.

18. The synchronous flash memory device of claim 17, wherein the interconnect pins are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

19. The synchronous flash memory device of claim 16, further comprising a package having a plurality of conductive interconnect locations corresponding to the command interface connections.

20. The synchronous flash memory device of claim 19, wherein the conductive interconnect locations are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

21. A computer system comprising:

a memory controller;

a main memory bus coupled to the memory controller; and

a synchronous non-volatile flash memory device coupled to the main memory bus, wherein the synchronous non-volatile flash memory device has a command interface comprising:

a write enable connection (WE#) to receive a write enable signal;

a column address strobe connection (CAS#) to receive a column address strobe signal;

a row address strobe connection (RAS#) to receive a row address strobe signal; and

a chip select connection (CS#) to receive a chip select signal.

22. The computer system of claim 21, wherein the synchronous non-volatile flash memory device comprises a package having a plurality of interconnect pins arranged in a manner that corresponds to interconnect pins of a synchronous dynamic random access memory device, wherein the plurality of interconnect pins of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) interconnect pins of the synchronous dynamic random access memory.

23. The computer system of claim 21, wherein the synchronous non-volatile flash memory device comprises a package having a plurality of solder bump connections arranged in a manner that corresponds to solder bump connections of a synchronous dynamic random access memory device, wherein the plurality of solder bump connections of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) solder bump connections of the synchronous dynamic random access memory.

24. The computer system of claim 21, wherein the synchronous non-volatile flash memory device comprises a plurality of external connections comprising:

a plurality of bi-directional data connections;

a plurality of memory address connections;

a clock input connection;

a clock enable connection;

a plurality of memory array bank address connections;

power supply connections;

a plurality of data mask connections;

a reset connection; and

a Vccp power supply connection.